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USPTO
19/841536
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	Subclass
	Class
	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E. <i>KS</i> SCANNED	PATENT DATE <i>T04 Q.A SW</i>
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/841536		712	34	2183	<i>Jan Ed Pan</i>
TITLE OF INVENTION: Sanjay Agarwal Sapna Agrawal					
Title: Coprocessor architecture for control processors using synchronous logic					
PTO-2040 1289					

ISSUING CLASSIFICATION					
ORIGINAL		CROSS REFERENCE(S)			
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
INTERNATIONAL CLASSIFICATION					
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket					

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <i>14</i>	Figs. Drwg.	Print Fig.	Total Claims <i>3</i>	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	(Primary Examiner)			ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	(Legal Instruments Examiner)			Amount Due	Date Paid
ISSUE BATCH NUMBER <i>[Signature]</i>					

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